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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/894,203	06/28/2001	Ichiro Tomohiro	299002053200	7078

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EXAMINER	
CERVETTI, DAVID GARCIA	
ART UNIT	**PAPER NUMBER**
2136	

DATE MAILED: 04/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/894,203	TOMOHIRO, ICHIRO	
	Examiner	Art Unit	
	David G. Cervetti	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 are pending and have been examined.

2. Applicant's arguments filed February 9, 2006, have been fully considered.

Response to Amendment

3. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Continued Examination Under 37 CFR 1.114

4. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114.

Claim Objections

5. Claims 7 and 8 are objected to because of the following informalities: "ROM" must be spelled out. Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Vicard (US Patent 5,708,715).

Regarding claim 1, Vicard teaches at least one non-volatile memory cell array block which is capable of receiving concurrent electrical erasure (column 2, lines 30-67, column 5, lines 1-67); a key means comprising a security release key (column 4, lines 20-67); a lock means comprising a security registration lock corresponding to each of the at least one memory cell array block (column 4, lines 20-67); at least one memory region, each one of said at least one memory region being provided in the at least one memory cell array block, for storing the security release key (column 5, lines 1-48); at least one non-volatile storage means for storing the security registration lock (column 5, lines 48-67, column 6, lines 1-36); a determination circuit for comparing a value which is generated based on the security release key against a value which is generated based on the security registration lock to determine whether or not to grant release of the security function (column 6, lines 1-67); and a memory cell array data output switching circuit for, when an output signal from the determination circuit indicates a matching result of comparison between the value which is generated based on the security release key and the value which is generated based on the security registration lock,

permitting data which is read from a corresponding one of the at least one memory cell array block to be externally output (column 6, lines 1-67).

Regarding claim 2, Vicard teaches the semiconductor storage device further comprises at least one register for retaining an output signal output from the determination circuit (column 5, lines 1-67); and when an output signal output from the at least one register indicates that release of the security function is to be granted, the memory cell array data output switching circuit permits data which is read from a corresponding one of the at least one memory cell array block to be externally output (column 6, lines 1-67).

Regarding claim 3, Vicard teaches instruction interpretation means for interpreting an externally-input setting instruction to write at least one of the security release key and the security registration lock into the at least one memory region or the at least one non-volatile storage means, respectively (column 6, lines 1-67).

Regarding claim 4, Vicard teaches wherein the determination circuit compares the value which is generated based on the security release key against the value which is generated based on the security registration lock for each of the at least one memory cell array block, and results of comparison are collaterally written in the at least one register (column 5, lines 1-67, column 6, lines 1-67).

Regarding claim 5, Vicard teaches a unidirectional conversion circuit or an encryption circuit, wherein results of converting the security release key and the security registration lock by means of the unidirectional conversion circuit or the encryption

circuit are written to the at least one memory region and the at least one non-volatile storage means, respectively (figures 1-3b, column 4, lines 20-67, column 5, lines 1-67).

Regarding claim 6, Vicard teaches which lacks means for reading the security release key and the security registration lock (column 6, lines 45-67, column 7, lines 1-8).

Regarding claim 7, Vicard teaches the at least one non-volatile storage means is a one-time programmable ROM which prohibits rewriting and erasure; and rewriting and erasure are prohibited after the security registration lock is written (column 5, lines 1-67, column 6, lines 1-36).

Regarding claim 8, Vicard teaches the at least one non-volatile storage means is a one-time programmable ROM which prohibits rewriting and erasure; and the semiconductor storage device has a non-volatile lock function for locking the semiconductor storage device to prohibit rewriting and erasure after writing of the security registration lock has been performed (column 5, lines 1-67, column 6, lines 1-36).

Regarding claim 9, Vicard teaches a flag indicating that the security release key has been set, wherein the flag is set automatically or manually after the security release key is written, thereby prohibiting additional writing to the corresponding one of the at least one memory cell array block (column 5, lines 25-67).

Regarding claim 10, Vicard teaches wherein a wait operation is performed while writing the security release key to the at least one memory region (column 6, lines 7-36).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David G. Cervetti whose telephone number is (571) 272-5861. The examiner can normally be reached on Monday-Friday 7:00 am - 5:00 pm, off on Wednesday.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R. Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DGC

CHRISTOPHER REVAK
PRIMARY EXAMINER

4/27/06